VERIFICATION OF TRANSLATION

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am the translator of the documents attached and I state that the following is a true translation to the best of my knowledge and belief of Japanese Patent Application No. 2003-132726.

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[NAME OF DOCUMENT] SPECIFICATION

[TITLE OF THE INVENTION] IMAGE DATA CONVERSION METHOD,

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CONVERTING CIRCUIT, AND ELECTRONIC CAMERA

[SCOPE OF CLAIMS]

[CLAIM 1]

A method for converting image data in a first format into image data in a second format, the image data in the first format having a first frame frequency and a first line frequency, the image data in the second format having a second frame frequency and a second line frequency, the method comprising:

retrieving every odd field period and every even field period in the second format, from a memory to which moving image data in the first format is written, respective signals required for producing image data of an odd field and an even field in the second format out of the image data in the first format;

converting the retrieved image data into first image data and second image data having a line frequency of the second format;

outputting the image data of the odd field in the second format by mixing image data of an odd field of the first image data and image data of an odd field of the second image data at a predetermined mixing ratio;

outputting the image data of the even field in the second format by mixing image data of an even field of the first image data and image data of an even field of the second image data at a predetermined mixing ratio; and

changing the mixing ratios every field period in the second format.

[CLAIM 2]

The method for converting image data according to claim 1,

wherein the first format is an NTSC format, and

wherein the second format is a PAL format.

[CLAIM 3]

The method for converting image data according to claim 1,

wherein the first format is an NTSC format, and

wherein the second format is switched to the NTSC format or a PAL format.

[CLAIM 4]

A converting circuit for image data for converting image data in a first

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format into image data in a second format, the image data in the first format having a first frame frequency and a first line frequency, the image data in the second format having a second frame frequency and a second line frequency, the converting circuit comprising:

a memory to which moving image data in the first format is written;

a first circuit retrieving every odd field period and every even field period in the second format, from the memory, respective signals required for producing image data of an odd field and an even field in the second format out of the image data in the first format;

a second circuit converting the retrieved image data into first image data and second image data having a line frequency in the second format;

a third circuit outputting the image data of the odd field in the second format by mixing image data of an odd field of the first image data and image data of an odd field of the second image data at a predetermined mixing ratio, and outputting the image data of the even field in the second format by mixing image data of an even field of the first image data and image data of an even field of the second image data at a predetermined mixing ratio; and

a fourth circuit changing the mixing ratios every field period in the second format.

[CLAIM 5]

The frame-converting circuit according to claim 4,

wherein the first format is an NTSC format, and

wherein the second format is a PAL format.

[CLAIM 6]

The frame-converting circuit according to claim 4,

wherein the first format is an NTSC format,

the frame-converting circuit further comprising

a circuit in which the second format is switched to the NTSC format or a PAL format.

[CLAIM 7]

An electronic camera in which image data in a first format has a first

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frame frequency and a first line frequency and image data in a second format has a second frame frequency and a second line frequency, the electronic camera comprising:

an image sensor that is projected with an image of an object and outputs the image data in the first format every frame period of the first format;

a memory to which the image data in the first format output from the image sensor is written;

a first circuit retrieving every odd field period and every even field period in the second format, from the memory, respective signals required for producing image data of an odd field and an even field in the second format out of the image data in the first format;

a second circuit converting the retrieved image data into first image data and second image data having a line frequency in the second format;

a third circuit outputting the image data of the odd field in the second format by mixing image data of an odd field of the first image data and image data of an odd field of the second image data at a predetermined mixing ratio, and outputting the image data of the even field in the second format by mixing image data of an even field of the first image data and image data of an even field of the second image data at a predetermined mixing ratio;

a fourth circuit changing the mixing ratios every field period in the second format; and

an external terminal outputting outwardly the image data output from the third circuit.

[CLAIM 8]

The electronic camera according to claim 7,

wherein the first format is an NTSC format,

the electronic camera further comprising

a circuit in which the second format is switched to the NTSC format or a PAL format.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

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[TECHNICAL FIELD TO WHICH THE INVENTION BELONGS]

The present invention relates to an electronic camera having a function of capturing and playing back moving images, in particular, to a technique of converting image data from an NTSC format into a PAL format.

[0002]

[PRIOR ART]

Many digital still cameras include LCD monitors for checking images to be captured and captured images.   In addition, many digital still cameras include video output terminals and can display images on, for example, external television receivers.

[0003]

Further, as a digital still camera, there is a type that can capture moving images in addition to still images.   In many cases, when capturing moving images, a digital still camera performs recording in an NTSC format in a VGA size (640 dots in width x 480 dots in height) in consideration of viewing on a personal computer (see Patent Documents 1, 2, and 3, for example).

[0004]

[Patent Document 1]

Japanese Patent Application Laid-open No. Hei 5-122663

[0005]

[Patent Document 2]

Japanese Patent Application Laid-open No. Hei 8-172609

[0006]

[Patent Document 3]

Japanese Patent Application Laid-open No. 2001-313896

[0007]

[PROBLEMS TO BE SOLVED BY THE INVENTION]

Incidentally, in a video camera (television camera), a CCD image sensor captures an image corresponding to one field period every field period, and image data corresponding to one field period is output from the CCD sensor every field period, as shown on the upper side of FIG. 7A.   The image data is then

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processed and output in series every field period from the camera as video signals, as shown on the lower side of FIG. 7A.

[0008]

It should be noted that in FIGS. 7, numerals 1, 2, 3, ... are serial numbers respectively assigned to arbitrary consecutive frames.   A symbol having a numeral with a suffix A indicates a number of an odd field in a frame indicated by that numeral, and a symbol with a suffix B indicates a number of an even field. In addition, solid arrows indicate image data flows of odd fields, and dotted arrows indicate image data flows of even fields (hereinafter, the same holds true for other drawings).

[0009]

However, originally, a digital still camera mainly captures still images and is capable of suitably capturing the still images.   Thus, in a digital still camera, a CCD image sensor captures an image one frame period at a time every frame period, and image data is output from the CCD image sensor one frame period at a time every frame period, as shown on the upper side of FIG. 7B.   The image data of one frame is split into image data of an odd field (solid arrow) and image data of an even field (dotted arrow) and output in series from the camera as video signals one field period at a time every field period, as shown on the lower side of FIG. 7B.

[0010]

The same capturing and outputting methods are used for capturing moving images.   Thus, when a digital still camera captures moving images, the motion of the images becomes jerky because the interval of capturing images is twice as that of a video camera.

[0011]

Synchronizing frequencies of the NTSC format and the PAL format and a frequency ratio thereof are as shown in FIG. 8.   Thus, when moving images are captured (or, moreover, recorded and played back) in the NTSC format, image data needs to undergo line conversion as well as frame conversion from the NTSC format to the PAL format so as to be viewed on a PAL television receiver.

[0012]

FIGS. 9 and 10 illustrate examples of the method for converting a frame. In this case, the upper sides of FIGS. 9 and 10 show image data before frame conversion which corresponds to, for example, image data as an output of a CCD image sensor or that has been recorded.   The lower sides show image data in the PAL format after frame conversion which corresponds to, for example, video signals output to an external television receiver from a camera or video signals supplied to a built-in LCD monitor.

[0013]

In the case of FIG. 9, a first frame to a third frame in the NTSC format are respectively used as they are for a first frame to a third frame in the PAL format, but the odd field in a fourth frame in the NTSC format is used as the odd field 4A in a fourth frame in the PAL format, and the even field is decimated.   A fifth frame in the NTSC format is used for the even field 4B in the fourth frame and the odd field 5A in a fifth frame in the PAL format.

[0014]

After that, fields in the NTSC format are decimated and converted into those in the PAL format so that the ratio of a frame frequency of the NTSC format to that of the PAL format of 1,200:1,001 is established.

[0015]

When every 1,200 frames of image data in the NTSC format are decimated to 1,001 frames, the sequence is complicated because the field to be decimated shifts as time elapses.   Thus, when executing under control of a CPU, there is a considerable software load.

[0016]

Thus, as shown in FIG. 10, each frame of image data is retrieved from a CCD image sensor or a recording medium every 1/30 seconds and converted into the PAL format.   In other words, in this case, the ratio of the frame frequency of the original image data to that of the PAL format of

30 Hz:25 Hz = 6:5

is obtained.   Accordingly, as shown in FIG. 10, image data in the PAL format

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can be obtained by decimating one frame in the NTSC format every six frames, thereby enabling an easy frame conversion.

[0017]

However, in this frame conversion method, considering a time axis, since information for one frame period every six frame periods in the NTSC format is dropped out, a discontinuous point occurs every five frames in the PAL format, which disables smooth playback.   In addition, when a digital still camera captures moving images, the motion of the images is jerky as compared with that of a video camera, as described above.   Hence, when frames of these moving images are converted with the technique shown in FIG. 10, the motion becomes jerkier.   Moreover, in some cases, an LCD monitor of a digital still camera does not support a 60 Hz synchronizing frequency system and display cannot be made with the LCD monitor.

[0018]

Moreover, because the number of horizontal lines of the NTSC format is different from that of the PAL format as shown in FIG. 8, when frames of the NTSC format are converted into those of the PAL format, in actuality, the number of horizontal lines also needs to be converted.   Thus, when image data in the NTSC format is converted into image data in the PAL format, both frame conversion and line conversion are carried out, but unless these conversions are suitably carried out, the whole converted image data lags behind by several frame periods.   A memory corresponding to these several frame periods also becomes necessary.

[0019]

The present invention is intended to solve the above problems.

[0020]

[MEANS FOR SOLVING THE PROBLEMS]

According to the present invention, there is provided a method for converting image data in a first format into image data in a second format, the image data in the first format having a first frame frequency and a first line frequency, the image data in the second format having a second frame frequency

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and a second line frequency, the method including:

retrieving every odd field period and every even field period in the second format, from a memory to which moving image data in the first format is written, respective signals required for producing image data of an odd field and an even field in the second format out of the image data in the first format;

converting the retrieved image data into first image data and second image data having a line frequency of the second format;

outputting the image data of the odd field in the second format by mixing image data of an odd field of the first image data and image data of an odd field of the second image data at a predetermined mixing ratio;

outputting the image data of the even field in the second format by mixing image data of an even field of the first image data and image data of an even field of the second image data at a predetermined mixing ratio; and

changing the mixing ratios every field period in the second format.

Thus, the image data in the first format is converted into the image data in the second format by mean value interpolation.

[0021]

[BEST MODE FOR CARRYING OUT THE INVENTION]

(1) Example of Digital Still Camera

FIG. 1 illustrates an example of a digital still camera 10 according to the present invention. An image of an object OBJ is projected onto a CCD image sensor 11 through an imaging lens LNS, three-primary-color image signals of the object OBJ are output from the image sensor 11 every frame period of the NTSC format, and the image signals are supplied to an A/D converter circuit 12 to be A/D-converted into digital image data.

[0022]

The image data is supplied to a camera signal-processing circuit 13 and converted into image data in a YUV format after being subjected to processes such as white balance correction and gamma correction, and the image data is then written to an area for display in a memory 16 by a memory controller 14 through an image bus 15. The area for display in the memory 16 constitutes a

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so-called video RAM, and addresses thereof respectively correspond to dot positions on a display screen.

[0023]

Then, the image data is read from the area for display in the memory 16 by the memory controller 14 in parallel with writing to the memory 16, and the read image data is supplied to a display signal-processing circuit 17 through the image bus 15 to be converted into image data in an RGB format, while being D/A-converted into analog image signals and supplied to an LCD panel 18 to be displayed as color images. Furthermore, in the display signal-processing circuit 17, color video signals are produced simultaneous with the analog image signals, and the video signals are output to an external video output terminal 19 to be supplied to a monitoring television receiver (not shown).

[0024]

The image data in the area for display in the memory 16 is also supplied to an image-companding circuit 21 by the memory controller 14 through the image bus 15 and is compressed into code data in a predetermined format, for example, a JPEG format, and the code data is temporarily written to a work area in the memory 16 through the image bus 15. Then, the code data written to the work area in the memory 16 is read by the memory controller 14, and the read code data is written to and stored in an external storage medium 23 such as a Memory Stick (registered trademark) by a microcomputer 22.

[0025]

At a time of playback, the code data is read from the external storage medium 23 by the microcomputer 22 and is temporarily written to the work area in the memory 16, the written code data is decompressed into the original image data by the image-companding circuit 21, and the decompressed image data is written to the area for display in the memory 16. Then, this written image data is processed by the display signal-processing circuit 17 to be displayed on the LCD panel 18 as color images and output to the external video output terminal 19 as color video signals, as described above.

[0026]

To smooth motions of moving images displayed on the LCD panel 18 and moving images of color video signals output to the external video output terminal 19 at times of image capturing and play back, the following signal processing is additionally carried out in the present invention.

[0027]

It should be noted that in the following description, if necessary, image data before frame conversion, such as the output of the CCD image sensor 11, is called "original image data", and image data and video signals after frame conversion, such as video signals output from the digital still camera 10, are respectively called "output image data" and "output video signals".

[0028]

(2) Capturing and Playing Back Moving Images

As shown on the upper side of FIG. 2, when moving images are captured, the CCD image sensor 11 is controlled so as to capture an image in the NTSC format one frame at a time every frame period and to output image data (original image data) one frame at a time every frame period. Thus, moving images stored in the external storage medium 23 and moving images read out are also in the NTSC format in frame units.

[0029]

According to the format of video signals (output video signals) supplied to LCD panel 18 or the external video output terminal 19, frame conversion and line conversion are carried out as follows.

[0030]

(2-1) Case of Extracting Video Signals in NTSC Format

As shown on the upper side of FIG. 2, original image data is obtained in units of frames in the NTSC format. However, in this case, since the original image data is extracted in the form of video signals in the NTSC format, the frame frequency and the line frequency of the output video signals are the same as those of the original image data.

[0031]

Accordingly, in this case, line conversion is not carried out, but frame

conversion as shown in FIG. 2 is carried out to suppress the jerkiness of the moving images.   Specifically, assuming that

DOUT: output image data and output video signals after frame conversion,

Dn: image data of odd field or even field in n-th frame in original image data,

Dn+1: image data of odd field or even field in (n+1)-th frame in original image data, and

KF: predetermined coefficient ($0 \leq KF \leq 1$),

the output image data DOUT is a signal component expressed by

$$DOUT = (1 - KF)Dn + KF*Dn+1 \ ... \ (1)$$

as shown in FIG. 2.

[0032]

It should be noted that when the output image data DOUT is that of the odd field, the original image data Dn and Dn+1 are image data of the odd fields, and when the image data DOUT is that of the even field, the original image data Dn and Dn+1 are image data of the even fields.   At this time, the coefficient KF is switched to, for example,

KF = 1/4 ... when the output image data DOUT is an odd field or

KF = 3/4 ... when the output image data DOUT is an even field

according to the field of the output image data DOUT.

[0033]

That is, fields of two continuous frames of the original image data are mixed at a predetermined ratio for each field while switching the ratio for each field period, to thus form the output image data (output video signals).

[0034]

In this way, even when the original image data is formed every frame period, since intermediate image data is formed by mean value interpolation every field period and display is made based on this formed image data, jerkiness of the moving images are suppressed.

[0035]

(2-2) Case of Extracting Video Signals in PAL Format

In this case, both the frame frequency and the line frequency of the original image data are different from those of the output image data. Thus, frame conversion and line conversion need to be carried out. As described below, lines of the original image data are converted first and frames of the image data after the line conversion are then converted to obtain the output image data.

[0036]

(2-2-1) Line Conversion

As shown in FIG. 8, since the ratio of the number of effective lines of the NTSC format to that of the PAL format is 5:6, five lines of the original image data are line-converted to six lines in the PAL format. In this regard, for example, this line conversion is carried out by mean value interpolation in the vertical direction, as shown in FIG. 3. Specifically, FIG. 3 shows the original image data and the image data after line conversion in units of horizontal lines. As shown on the left-hand side of FIG. 3, the original image data has a horizontal line period of the NTSC format. It should be noted that a number assigned to each line indicates a line number in each frame period. Moreover, solid lines indicate horizontal lines of the odd field, and dotted lines indicate horizontal lines of the even field.

[0037]

(A) As shown on the right-hand side of FIG. 3, the first line and the second line of the original image data are mixed in a ratio of 1:11 to generate a first line after line conversion, that is, a first line of an odd field after the conversion.

(B) As shown on the right-hand side of FIG. 3, the second line and the third line of the original image data are mixed in a ratio of 3:9 to generate a second line after line conversion, that is, a first line of an even field after the conversion.

(C) The third line and the fourth line of the original image data are mixed in a ratio of 5:7 to generate a third line after line conversion, that is, a second line of an odd field after the conversion.

(D) The fourth line and the fifth line of the original image data are mixed in a ratio of 7:5 to generate a fourth line after line conversion, that is, a second line of

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an even field after the conversion.

(E) The fifth line and the sixth line of the original image data are mixed in a ratio of 9:3 to generate a fifth line after line conversion, that is, a third line of an odd field after the conversion.

(F) The sixth line and the seventh line of the original image data are mixed in a ratio of 11:1 to generate a sixth line after line conversion, that is, a third line of an even field after the conversion.

After that, the same processes as (A) to (F) are repeated every five lines of the original image data.

[0038]

Specifically, assuming that

dOUT: output image data after line conversion,

dm: image data of m-th line in original image data,

dm+1: image data of (m+1)-th line in original image data, and

KL: predetermined coefficient ($0 \leq KL \leq 1$),

the image data dOUT after line conversion is a signal component expressed by

$$dOUT = (1 - KL)dm + KL*dm+1 \ ... \ (2)$$

as shown in FIG. 3.

[0039]

It should be noted that at this time, regarding the coefficient KL, for example,

· when the image data dOUT after the conversion is the odd field,

11/12, 7/12, and 3/12

are repeated in a field order.

· When the image data dOUT after the conversion is the even field,

9/12, 5/12, and 1/12

are repeated in the field order.

[0040]

That is, two continuous lines of the original image data that are temporally closest to the converted image data dOUT are mixed at a predetermined ratio, and the ratio is switched every horizontal line period of the

resultant image data for mixture to form image data having as many lines as in the PAL format.

[0041]

In this way, even when the number of effective lines of the original image data is 480, image data having 576 effective lines in the PAL format can be generated by mean value interpolation of image data of an intermediate line.

[0042]

(2-2-2) Frame Conversion

This frame conversion is for converting the image data line-converted according to expression (2) into output image data in the PAL format, but is realized by mean value interpolation as shown in FIGS. 4A and B. Here, FIG. 4A shows the image data line-converted according to expression (2) in units of frames, and FIG. 4B shows the output image data after frame conversion in units of frames.

[0043]

That is, this frame conversion also generates output image data DOUT according to expression (1). It should be noted that in this case, image data Dn and Dn+1 are image data DOUT (= Dn) and DOUT (= Dn+1), respectively, of two fields line-converted according to expression (2). Moreover, the coefficient KF changes by a predetermined amount every field period of the output image data DOUT according to a frame shift between the image data after the line conversion and the output image data DOUT.

[0044]

That is, image data (image data after line conversion) of two continuous fields that are temporally closest to the image data DOUT after the frame conversion are mixed at a predetermined ratio, and the ratio is switched every field period according to the shift with respect to the image data after the frame conversion for mixture to thus obtain image data in the PAL format.

[0045]

Thus, since image data at a field position in the PAL format is generated by mean value interpolation even when the image data after the line conversion

has a frame period of the NTSC format, jerkiness in motions of the moving images can are suppressed when display is made based on this image data after the frame conversion.

[0046]

(3) Example of Circuit for Producing Output Image Data from Original Image Data

Processing of line-converting and frame-converting the original image data into output image data (output video signals) is executed mainly by, for example, the memory controller 14 and the display signal-processing circuit 17, as shown in FIG. 5. It should be noted that hereinafter, a case where output image data is image data in the PAL format will mainly be described. Further, the original image data is written to the memory 16 in a bit map corresponding to the display screen, and the original image data is read out from addresses corresponding to respective horizontal scanning positions.

[0047]

As is apparent from FIG. 8, a length of 1,200 frame periods of the NTSC format is the same as that of 1,001 frame periods of the PAL format. A shift between a frame of the NTSC format and a frame of the PAL format circuits every time this period passes.

[0048]

Therefore, the display signal-processing circuit 17 includes signal-generating circuits 171 and 172 that generate various types of timing signals. The signal-generating circuit 171 outputs a pulse NTFRM of a frame period of the NTSC format as shown in FIG. 4D as well as a pulse RSTRT every 1,200 frames of the NTSC format as shown in FIG. 4C.

[0049]

Moreover, the signal-generating circuit 172 outputs a pulse FLDPLS and a rectangular-wave signal FLDRCT of a field period of the NTSC format or a field period of the PAL format as shown in FIGS. 4E and F. The microcomputer 22 supplies predetermined control signals to the signal-generating circuit 172 to set the period of the pulses FLDPLS and signals FLDRCT to the NTSC field

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period or the PAL field period.   The signal-generating circuit 172 is also supplied with the pulses RSTRT from the signal-generating circuit 171.

[0050]

Furthermore, since the original image data is read out from addresses of the memory 16 corresponding to respective horizontal scanning positions, the memory controller 14 includes two sets of registers (latch circuits) 141 to 143 and 144 to 146, an address counter 149, and the like.

[0051]

In this case, the registers 141 to 143 store an odd-field start address (start address of first odd line) A_STAD, and the registers 144 to 146 store data ADDNUM indicating the number of addresses (number of pixels) per line.   The count value of the address counter 149 is used as a readout address of the memory 16, and the readout address (count value) changes from the start address by counting of a predetermined clock.

[0052]

When the microcomputer 22 supplies the odd-field start address A_STAD and a clock CK to the register 141, the start address A_STAD is retained by the register 141, and an output from the register 141 and the pulses NTFRM from the signal-generating circuit 171 are supplied to the register 142 so that the odd-field start address A_STAD is retained by the register 142. Furthermore, an output from the register 142 and the pulses FLDPLS from the signal-generating circuit 172 are supplied to the register 143, and the odd-field start address A_STAD is output from the register 143 every pulse FLDPLS.

[0053]

Similarly, the microcomputer 22 supplies the data ADDNUM indicating the number of addresses per line to the register 144, and the data ADDNUM is extracted from the register 146.

[0054]

An adding circuit 147 adds the odd-field start address A_STAD output from the register 143 and the data ADDNUM indicating the number of addresses per line output from the register 146, and an even-field start address (start address

of first even line) B_STAD is extracted from the adding circuit 147.

[0055]

Then, the odd-field start address A_STAD and the even-field start address B_STAD are supplied to a data selector 148, and the signals FLDRCT from the signal-generating circuit 172 are supplied to the data selector 148 as control signals (in this case, the signals FLDRCT are inverted every PAL field period). Thus, as shown in FIG. 4G, the data selector 148 alternately extracts the odd-field start address A_STAD and the even-field start address B_STAD every PAL field period.

[0056]

These start addresses extracted from the data selector 148 are supplied to the address counter 149, and a count value thereof is supplied to the memory 16 as a readout address. Thus, the original image data is extracted from the memory 16 every PAL field period.

[0057]

The extracted original image data is then alternately supplied to a pair of line-interpolating circuits 73 and 74 provided in the display signal-processing circuit 17 every frame period. The line-interpolating circuits 73 and 74 convert lines of the original image data by interpolation according to expression (2). Therefore, the line-interpolating circuit 73 includes a converting circuit 731 and arithmetic circuits 732 to 734, and the line-interpolating circuit 74 includes a converting circuit 741 and arithmetic circuits 742 to 744.

[0058]

In this case, the converting circuit 731 includes a buffer memory (not shown) and synchronously outputs image data dm of the m-th line and image data dm+1 of the (m+1)-th line in the n-th frame out of the original image data read out from the memory 16.

[0059]

Then, these synchronized image data dm and dm+1 are supplied to the subtracting circuit 732, which subtracts the data dm from the data dm+1, and the subtraction result (dm+1 - dm) is supplied to the multiplying circuit 733. At the

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same time, the coefficient KL is supplied to the multiplying circuit 733 from a coefficient-generating circuit 76 as will be described later and multiplied to the value (dm+1 - dm). Then, the multiplication result KL(dm+1 - dm) is supplied to the adding circuit 734, and the data dm from the converting circuit 731 is also supplied to the adding circuit 734.

[0060]

Therefore, the adding circuit 734 outputs the image data dOUT expressed by

$$KL(dm+1 - dm) + dm = (1 - KL)dm + KL*dm+1$$
$$= dOUT \ldots (3)$$

That is, the line-converted image data dOUT is obtained for the n-th frame. This image data dOUT is used as image data Dn of the n-th frame in expression (1), and is therefore (line-converted) image data Dn hereinafter.

[0061]

Further, the structure of the line-interpolating circuit 74 is similar to that of the line-interpolating circuit 73, except that the converting circuit 741 synchronously outputs image data dm of the m-th line and image data dm+1 of the (m+1)-th line in the (n+1)-th frame out of the original image data read out from the memory 16.

[0062]

Thus, the image data dOUT line-converted for the (n+1)-th frame can be obtained from the adding circuit 744 in the line-interpolating circuit 74. This image data dOUT is image data obtained one frame period after the image data Dn (= dOUT) output from the line-interpolating circuit 73 and is thus (line-converted) image data Dn+1 of the (n+1)-th frame in expression (1). Therefore, line-converted image data of two continuous frames are synchronously output from the line-interpolating circuits 73 and 74.

[0063]

After that, these line-converted image data Dn and Dn+1 are supplied to a frame-interpolating circuit 75 provided in the display signal-processing circuit 17. The frame-interpolating circuit 75 is for converting frames of the

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line-converted image data Dn and Dn+1 into those of output image data by interpolation according to expression (1).

[0064]

Therefore, the line-converted image data Dn and Dn+1 are supplied to a subtracting circuit 752 that subtracts the data Dn from the data Dn+1, and the subtraction result (Dn+1 - Dn) is supplied to a multiplying circuit 753. At the same time, the coefficient KF is supplied to the multiplying circuit 753 from a coefficient-generating circuit 77 to be described later and multiplied to the value (Dn+1 - Dn). Then, the multiplication result KL(Dn+1 - Dn) is supplied to an adding circuit 754, and the data Dn from the converting circuit 751 is also supplied to the adding circuit 754.

[0065]

Therefore, the adding circuit 754 outputs the image data DOUT expressed by

$$KF(Dn+1 - Dn) + Dn = (1 - KF)Dn + KF*Dn+1$$
$$= DOUT \ldots (4)$$

That is, the image data DOUT subjected to the frame conversion and line conversion is obtained.

[0066]

Then, this image data DOUT is D/A-converted to analog color video signals and output to the external video output terminal 19. Thus, images are displayed in the PAL format on a monitoring television receiver connected to the external video output terminal 19.

[0067]

(4) Example of Coefficient-Generating Circuits 76 and 77

As described above, the coefficient-generating circuit 76 generates the coefficient KL for line conversion, and the coefficient-generating circuit 77 generates the coefficient KF for frame conversion. Therefore, main parts of the coefficient-generating circuits 76 and 77 can be made the same as shown in FIG. 6, for example. In this regard, in descriptions below, the coefficient-generating circuit 77 for frame conversion having a simple structure and processing content

will first be described.

[0068]

(4-1) Example of Coefficient-Generating Circuit 77

The coefficient-generating circuit 77 generates a coefficient KF which changes according to a shift between the NTSC frame and the PAL frame, but in this example, when output image data in the PAL format is formed based on image data after line conversion, resolution of time positions of the output image data is 1/128 the field period of the PAL format.

[0069]

The coefficient-generating circuit 77 includes a data selector 771 that switches the initial value and the delta value, an adding circuit 772 for accumulation, and 7-bit register (a latch circuit) 773 that stores the accumulated value.   Further, the microcomputer 22 outputs, for example, "0" and "76" as the initial value and the delta value, respectively, so as to supply them to the data selector 771 and the adding circuit 772.   Furthermore, the signal-generating circuit 171 supplies the pulses RSTRT to the data selector 771 as control signals.

[0070]

When RSTRT = "1", the initial value "0" is extracted from the data selector 771, and the register 773 stores the extracted initial value "0" by the pulse FLDPLS from the signal-generating circuit 172.   Thus, as shown in FIG. 4H, an output QF of the register 773 is "0" during one field period (period of field 1A) since the pulse RSTRT.   Further, at this time, the output QF (= 0) of the register 773 and the delta value "76" from the microcomputer 22 are summed up in the adding circuit 772, and the summed-up value "76" is output from the adding circuit 772.

[0071]

Subsequently, since, when the value of RSTRT becomes "0" and one field period has elapsed, RSTRT becomes "0" at a point after the elapse (start point of field 1B), the output from the adding circuit 772, that is, the value "76" in this case is supplied to the register 773 through the data selector 771, and the register 773 stores it by the pulse FLDRCT.   Therefore, as shown in FIG. 4H, QF

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becomes 76 from this point in time. Moreover, the output of the adding circuit 772 consequently becomes "152".

[0072]

Upon elapse of an additional field period of the PAL format, the output "152" of the adding circuit 772 is supplied to the register 773 through the data selector 771, and the register 773 stores it by the pulse FLDRCT. It should be noted that at this time, since the register 773 is a 7-bit register, only the lower 7 bits of the output "152" of the adding circuit 772 are latched into the register 773, and the output QF of the register 773 becomes "24" (= 152 - 128) as shown in FIG. 4H.

[0073]

Since the operation as described above is repeated every field period of the PAL format thereafter, the output QF of the register 773 changes every field period of the PAL format, as shown in FIG. 4H. Then, this output QF is shifted only by 7 bits in an LSB direction to become a value QF/128, and this value is supplied to the multiplying circuit 753 in the frame-interpolating circuit 75 as the coefficient KF. It should be noted that when both sides of expression (1) are multiplied by 128,

$$128 \times DOUT = 128 \times (1 - KF)Dn + 128 \times KF \times Dn+1$$
$$= (128 - QF)Dn + QF*Dn+1 \ ...(5)$$

is obtained.

[0074]

Thus, since QF = 0 (KF = 0) for the period of the odd field 1A in the first frame of the output image data, image data of the odd field 1A is formed by mixing the odd field in the first frame and the odd field in the second frame of the image data after the line conversion at a ratio of 128:0, as shown in FIG. 4I. Since QF = 76 (KF = 76/128) for the period of the even field 1B in the first frame of the output image data, image data of the even field 1B is formed by mixing the even field in the first frame and the even field in the second frame of the image data after the line conversion at a ratio of 52:76.

[0075]

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Furthermore, since QF = 24 (KF = 24/128) for the period of the odd field 2A in the second frame of the output image data, image data of the odd field 2A is formed by mixing the odd field in the second frame and the odd field in the third frame of the image data after the line conversion at a ratio of 104:24. Further, since QF = 100 (KF = 100/128) for the period of the even field 2B in the second frame of the output image data, image data of the even field 2B is formed by mixing the even field in the second frame and the even field in the third frame of the image data after the line conversion at a ratio of 28:100.

[0076]

After that, image data of fields of two continuous frames of the image data after the line conversion are similarly mixed at a ratio as shown in FIG. 4I every field period of the PAL format to form the output image data DOUT (output video signals).

[0077]

Thus, even when the image data after the line conversion is in the frame period of the NTSC format, image data at a field position when captured in the PAL format is formed by mean value interpolation, and the formed image data becomes the output image data DOUT, with the result that jerkiness at a time moving images are captured is suppressed and motions become smooth.

[0078]

On the other hand, when obtaining the output image data DOUT in the NTSC format, the microcomputer 22 controls the signal-generating circuit 172 so as to set the period of the pulses FLDPLS and that of the signals FLDRCT to be the NTSC field period. The microcomputer 22 outputs, for example, "32" and "64" to the data selector 771 and the adding circuit 772 as the initial value and the delta value, respectively. Moreover, KL is set to, for example, 0.

[0079]

Therefore, in this case, since the output QF of the coefficient-generating circuit 77 is alternately switched to "32" or "96" every field period of the NTSC format, the coefficient KF to be the mixing ratio in the interpolating circuit 77 is alternately switched to 1/4 or 3/4 every field period of the NTSC format. Thus,

since the process is as shown in FIG. 2, moving images having smooth motions can be displayed also when the output image data DOUT in the NTSC format is obtained.

[0080]

(4-2) Example of Coefficient-Generating Circuit 76

The coefficient KL generated by the coefficient-generating circuit 76 is used for mixing two continuous lines of image data at, for example, ratios shown in FIG. 3. Thus, as shown in FIG. 6, the structure of the coefficient-generating circuit 76 is basically the same as that of the coefficient-generating circuit 77.

[0081]

That is, the coefficient-generating circuit 76 includes a data selector 761, an adding circuit 762, and a register 763 respectively corresponding to the data selector 771, the adding circuit 772, and the register 773 in the coefficient-generating circuit 77, a data selector 764, and a detecting circuit 765. In this case, the detecting circuit 765 is supplied with the pulses FLDPLS, a summed output from the adding circuit 762, and an output QL from the register 763 and detects a start point of each field period in the output image data, which is a start point of the field period of the PAL format in this case, and the detection output is supplied to the selector 761 as control signals.

[0082]

To align spatial positions of horizontal lines of the odd field and the even field in the output image, the initial value A_OFF of the odd field and the initial value B_OFF of the even field are extracted from the microcomputer 22. The initial value A_OFF is a value corresponding to a mixing ratio of 1:11 for mixing the first line and the second line in FIG. 3 (A) above, and the initial value B_OFF is a value corresponding to a mixing ratio of 3:9 for mixing the second line and the third line in FIG. 3 and (B) above.

[0083]

Then, the data selector 764 is supplied with these initial values A_OFF and B_OFF and the rectangular-wave signals FLDRCT from the signal-generating circuit 172 are also supplied to the data selector 764 as control

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signals, and the initial values A_OFF and B_OFF are extracted from the data selector 764 every relevant field period.

[0084]

The extracted initial value A_OFF or B_OFF is supplied to the data selector 761 and a delta value LPHASE is output from the microcomputer 22 to be supplied to the adding circuit 762.   In this case, the delta value LPHASE corresponds to the delta value 2/11 of the mixing ratio shown in FIG. 3.   The signal-generating circuit 172 supplies a predetermined latch pulse to the register 763 at the start point of every horizontal line period of the output image data.

[0085]

Thus, the value QL of the register 763 is set to the initial value A_OFF or B_OFF at the start point of every field period of the output image data and subsequently becomes a value obtained by adding the delta value LPHASE every horizontal line period.   Therefore, the value QL changes as shown in FIG. 3.   In this regard, the value QL is supplied as the coefficient KL to the multiplying circuit 733 in the line-interpolating circuit 73 and the multiplying circuit 743 in the line-interpolating circuit 74, where line conversion is carried out.

[0086]

(5) Summary

According to the above digital still camera, since image data temporally positioned at a field position of the PAL format is formed by mean value interpolation when frames of image data in the NTSC format are converted into those in the PAL format and the formed image data is used as display signals, moving images with smooth motions can be displayed.

[0087]

Also when lines in the NTSC format are converted to those in the PAL format, image data temporally positioned at a line position in the PAL format is formed by mean value interpolation, high quality images can be obtained without causing nonuniformity in lines on a display screen.

[0088]

Furthermore, as is apparent from FIGS. 3 and 4, since line conversion

and frame conversion can be carried out upon obtaining two frames of original image data, a delay of image data due to the line conversion and frame conversion is about two frame periods, with the result that a delay of output image data can be suppressed.   Moreover, a memory capacity can consequently be reduced.

[0089]

It should be noted that in the above descriptions, if the line conversion coefficient KL and the frame conversion coefficient KF are changed, application is also possible with respect to conversion of image data having other horizontal line frequencies and frame frequencies.

[0090]

[LIST OF ABBREVIATIONS USED IN SPECIFICATION]

A/D: Analog to Digital

CCD: Charge Coupled Device

CPU: Central Processing Unit

JPEG: Joint Photographic Experts Group

LCD: Liquid Crystal Display

LSB: Least Significant Bit

NTSC: National Television System Committee

PAL: Phase Alternation by Line

RGB: Red, Green and Blue

VGA: Video Graphics Array

YUV: Y-signal, U-signal and V-signal

[0091]

[EFFECT OF THE INVENTION]

According to the present invention, since line conversion and frame conversion of image data in an NTSC format into image data in a PAL format are realized by spatial and temporal mean value interpolation, high quality moving images having smooth motions can be obtained.   Furthermore, a delay of image data due to the line conversion and frame conversion is about two frame periods, thereby suppressing a delay of output image data.   Moreover, a memory capacity

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can consequently be reduced.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIG. 1]

A system diagram illustrating an embodiment of the present invention.

[FIG. 2]

A diagram for explaining the present invention.

[FIG. 3]

A diagram for explaining the present invention.

[FIGS. 4]

Diagrams for explaining the present invention.

[FIG. 5]

A system diagram illustrating a part of the present invention.

[FIG. 6]

A system diagram illustrating a part of the present invention.

[FIGS. 7]

Diagrams for explaining the present invention.

[FIG. 8]

A diagram for explaining the present invention.

[FIG. 9]

A diagram for explaining the present invention.

[FIG. 10]

A diagram for explaining the present invention.

[DESCRIPTION OF REFERENCE NUMERALS]

10 ... digital still camera, 11 ... CCD image sensor, 12 ... A/D converter circuit, 13 ... camera signal-processing circuit, 14 ... memory controller, 15 ... image bus, 16 ... memory, 17 ... display signal-processing circuit, 18 ... LCD panel, 19 ... external video output terminal, 21 ... image-companding circuit, 22 ... microcomputer, 23 ... external storage medium, 73 and 74 ... line-interpolating circuit, 76 and 77 ... coefficient-generating circuit, 141 to 146, 763, and 773 ... register, 148, 761, 764, and 771 ... data selector, 171 and 172 ... signal-generating circuit

【書類名】図面

【図1】

【図2】

【図3】

ライン変換後の画像データ（ＰＡＬのライン数）

1水平期間（ＰＡＬ）

原画像データ（ＮＴＳＣ）

1水平期間（ＮＴＳＣ）

Application No. 2003-132726

【図４】

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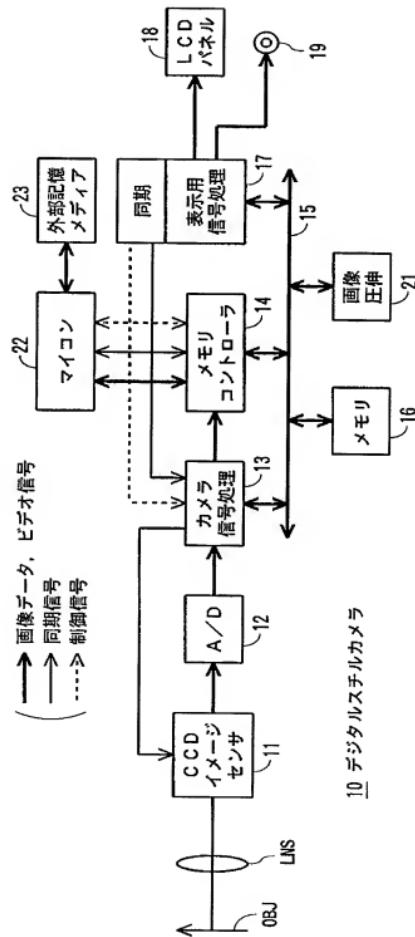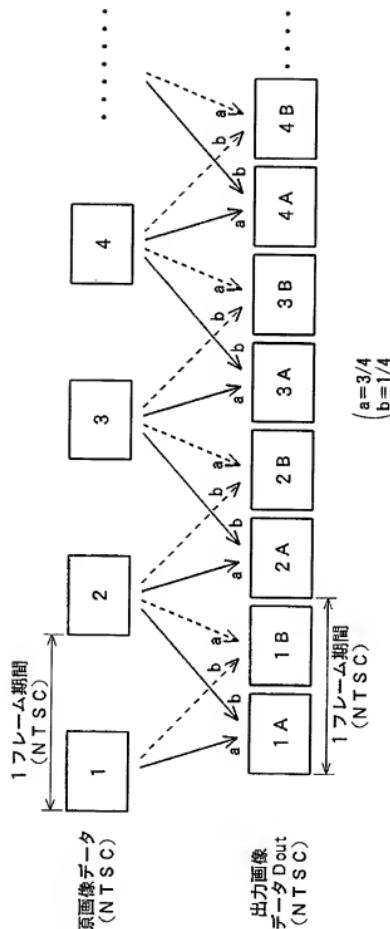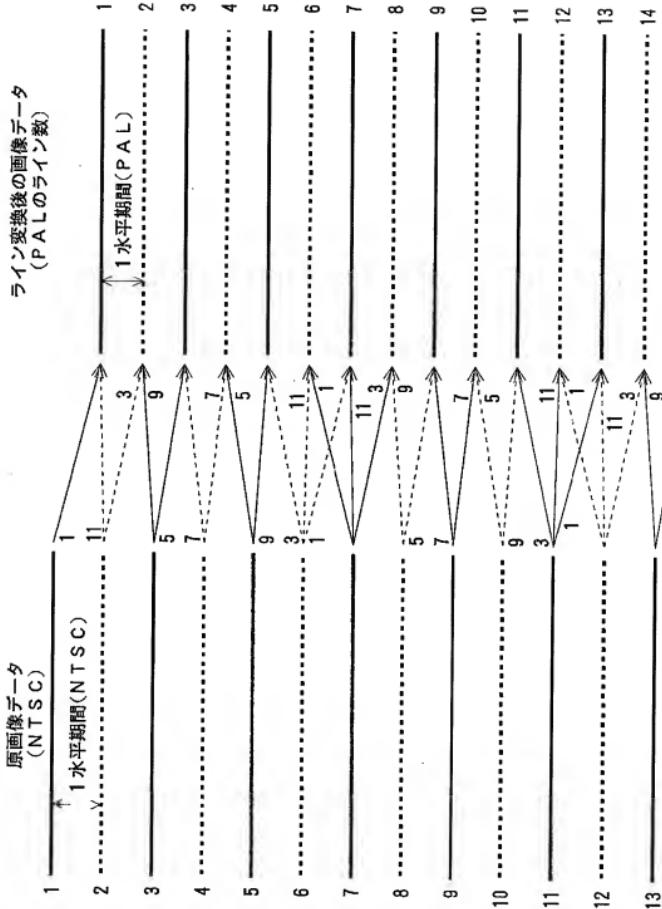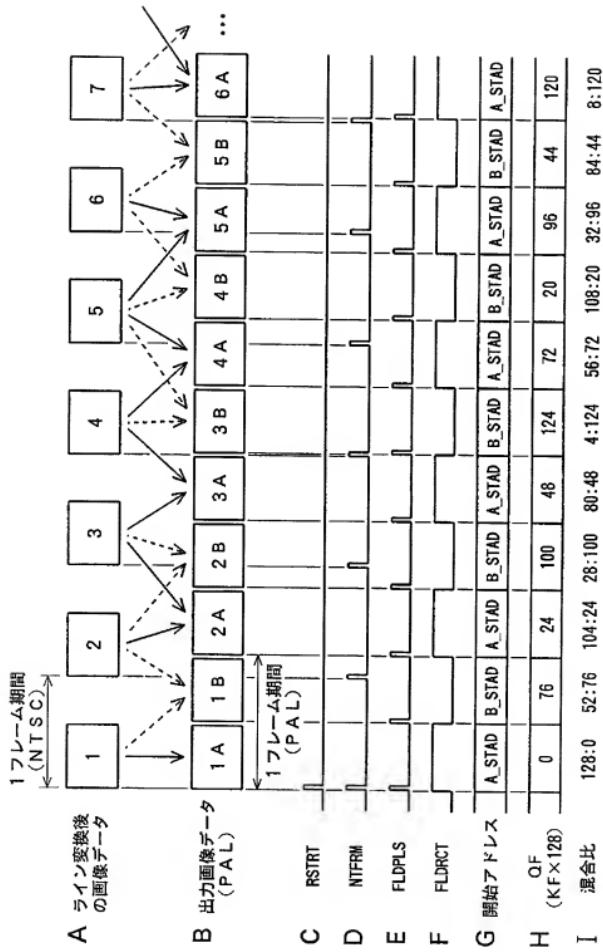
【図5】
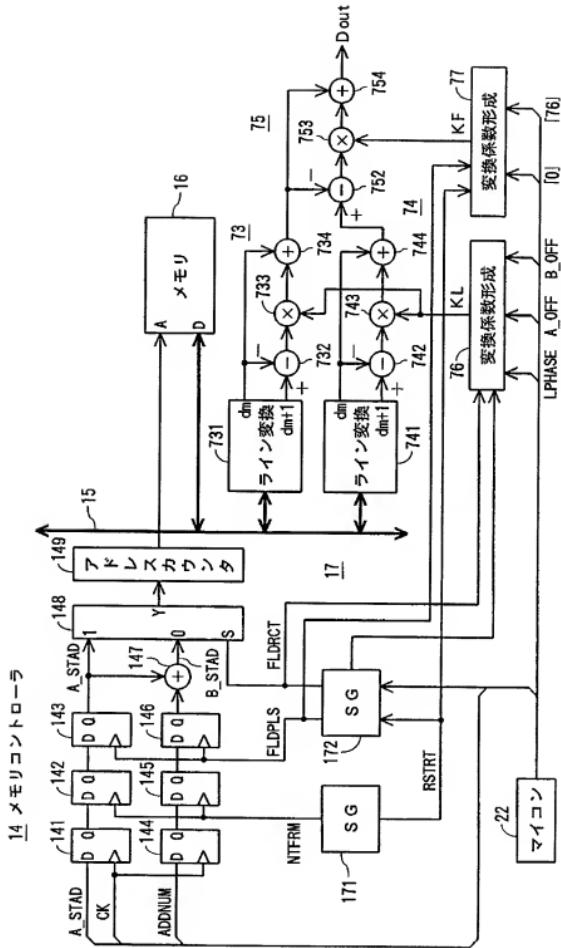
【図6】
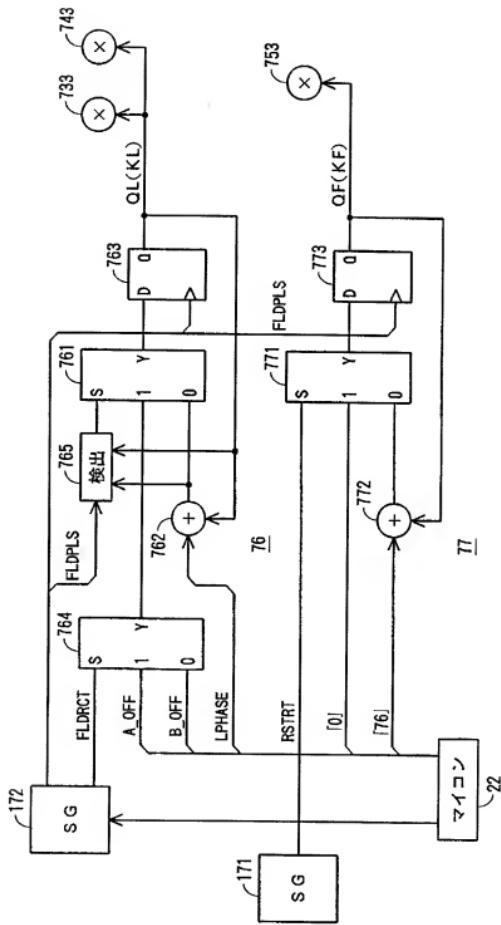
【図7】
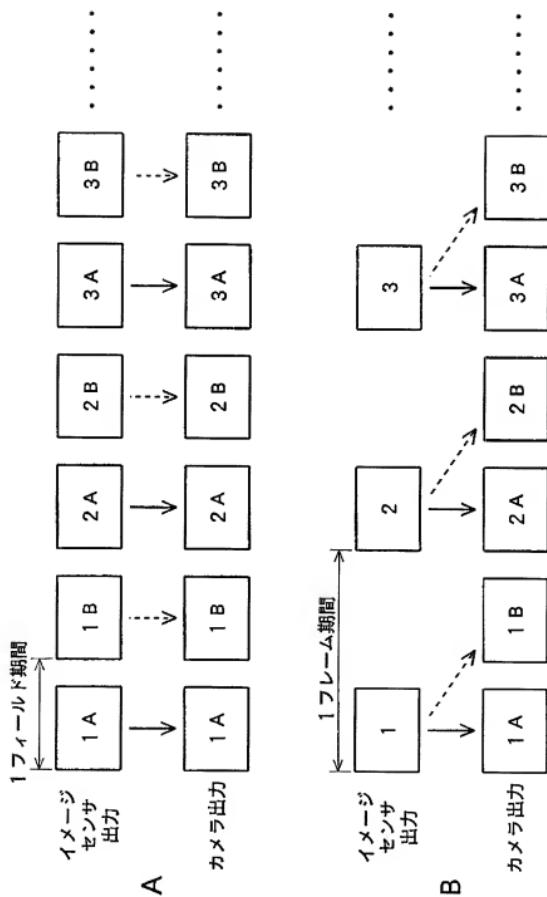
【図8】

	ＮＴＳＣ	ＰＡＬ
水平ライン数	525本	625本
有効ライン数	480本程度	576本程度
水平周波数ｆｈ	4.5MHz／286 ≒15.734kHz	4.5MHz／288 ＝15.625kHz
フレーム周波数	ｆｈ／525 ≒29.97Hz	ｆｈ／625 ＝25Hz
フィールド周波数	2ｆｈ／525 ≒59.94Hz	2ｆｈ／625 ＝50Hz

ＮＴＳＣ方式のフレーム周波数 ： ＰＡＬ方式のフレーム周波数

$$= \frac{4.5MHz}{286} \div 525 : \frac{4.5MHz}{288} \div 625$$

$$= 1200 : 1001$$

$$\fallingdotseq 6 : 5$$

ＮＴＳＣ方式の有効ライン数 ： ＰＡＬ方式の有効ライン数

$$\fallingdotseq 480本 : 576本$$

$$= 5 : 6$$

【図9】
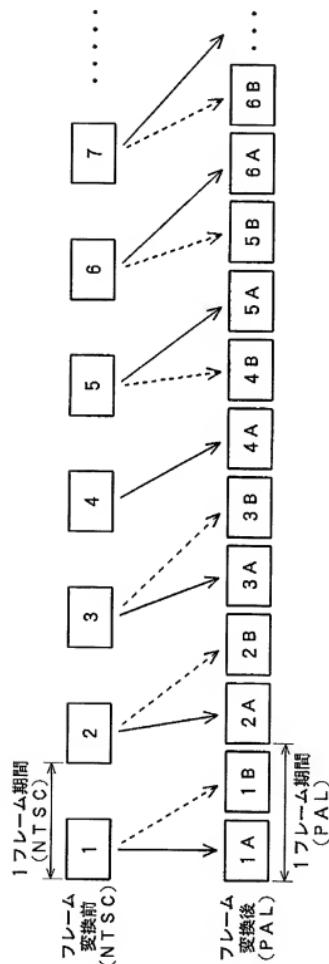
【図１０】
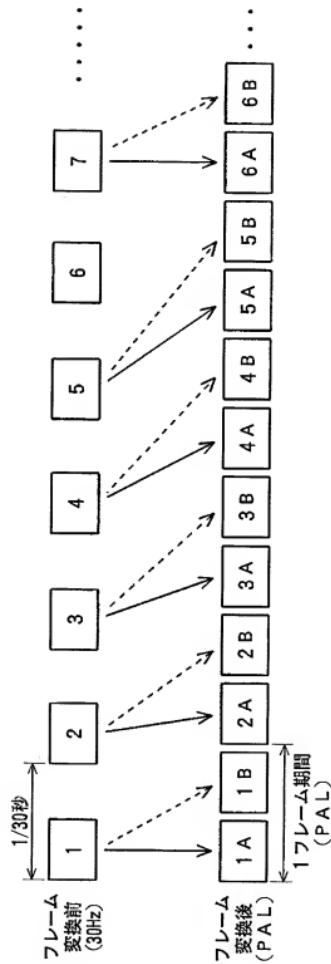
【書類名】図面	[NAME OF DOCUMENT] DRAWINGS	
【図1】	FIGURE 1	
10	Digital still camera	
11	CCD image sensor	
13	Camera signal processing	
14	Memory controller	
16	Memory	
17	Display signal processing	
18	LCD panel	
21	Image companding	
22	Microcomputer	
23	External storage medium	
同期	Synchronizing	
画像データ、ビデオ信号	Image data, video signal	
同期信号	Synchronizing signal	
制御信号	Control signal	
【図2】	FIGURE 2	
1フレーム期間	One frame period	
原画像データ	Original image data	
出力画像データDout	Output image data Dout	
【図3】	FIGURE 3	
原画像データ	Original image data	
1水平期間	One horizontal period	

Line numbers in left margin: 5, 10, 15, 20, 25

ライン変換後の画像データ	Image data after line conversion
（ＰＡＬのライン数)	Number of lines in PAL

【図4】 FIGURES 4

1フレーム期間	One frame period
ライン変換後の画像データ	Image data after line conversion
出力画像データ	Output image data
開始アドレス	Start address
混合比	Mixing ratio

【図5】 FIGURE 5

14	Memory controller
16	Memory
22	Microcomputer
76	Conversion coefficient generating
77	Conversion coefficient generating
149	Address counter
731	Line converting
741	Line converting

【図6】 FIGURE 6

22	Microcomputer
765	Detecting

【図7】 FIGURES 7

1フィールド期間	One field period

イメージセンサ出力	Image sensor output
カメラ出力	Camera output
1フレーム期間	One frame period

5 【図8】 FIGURE 8

水平ライン数	Number or horizontal lines
有効ライン数	Number of effective lines
水平周波数	Horizontal frequency
フレーム周波数	Frame frequency
10 フィールド周波数	Field frequency
525本	525 lines
625本	625 lines
480本程度	About 480 lines
576本程度	About 576 lines

15 ＮＴＳＣ方式のフレーム周波数：ＰＡＬ方式のフレーム周波数

Frame frequency of NTSC format: Frame frequency of PAL format

ＮＴＳＣ方式の有効ライン数：ＰＡＬ方式の有効ライン数

Number of effective lines of NTSC format: Number of effective lines of PAL format

20 480本：576本　480 lines: 576 lines

【図9】 FIGURE 9

1フレーム期間　One frame period

フレーム変換前	Before frame conversion
フレーム変換後	After frame conversion

【図１０】	FIGURE 10
1/３０秒	1/30 second
１フレーム期間	One frame period
フレーム変換前	Before frame conversion
フレーム変換後	After frame conversion

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[NAME OF DOCUMENT] ABSTRACT

[SUMMARY]

[OBJECT]   To provide a circuit for converting a format of image data having smooth motions.

5   [SOLVING MEANS]   A memory 16 to which moving image data in an NTSC format is written and a circuit 14 for extracting from the memory 16 respective signals required for producing image data of an odd field and an even field in a PAL format are provided.   Circuits 73 and 74 for converting the extracted image data into first and second image data having a line frequency of the PAL format

10   are provided.   A circuit 75 for outputting image data of an odd field in the PAL format by mixing image data of odd fields in the first and second image data at a predetermined ratio, and outputting image data of an even field in the PAL format by mixing image data of even fields at a predetermined ratio, and a fourth circuit 77 for changing the mixing ratios every field period in the PAL format are

15   provided.

[SELECTED DRAWING] Figure 5